IN THE CLAIMS:

1. (currently amended) An integrated circuit having complementary metal oxide semiconductor (CMOS) transistors including a p-type field effect transistor (PFET) and an n-type field effect transistor (NFET), each said NFET and said PFET having a channel region disposed in a single-crystal layer of a first semiconductor, wherein a stress is applied at a first magnitude to a channel region of said PFET but not to a channel region of said NFET by a layer of a second semiconductor which is lattice-mismatched to said first semiconductor, said layer of said second semiconductor being formed in source and drain regions of said PFET a first distance from said channel region of said PFET, and said layer of said second semiconductor further being formed in source and drain regions of said NFET at a second distance from said channel region of said NFET, said second distance being greater than said first distance.

2. (currently amended) The integrated circuit of claim 1 wherein said first semiconductor and said second semiconductor are silicon containing semiconductor materials having a composition according to the formula Si_xGe_y, wherein x and y are percentages, said first semiconductor ranging in composition between ~~xyto xy~~x = 100, y = 0 to x =1, y = 99, and said second semiconductor ranging in composition between ~~xyto xy~~x = 99, y = 1 to x =1, y = 99, wherein ~~y-~~x for said second semiconductor is always ~~greater~~ less than ~~y-~~x for said first semiconductor.

3. (original) The integrated circuit of claim 1 wherein said single-crystal region of said first semiconductor has a main surface defined by a level of a gate dielectric formed on said channel regions of said NFET and said PFET and said layer of said second semiconductor is formed above said main surface.

4. (original) The integrated circuit of claim 3 further comprising a layer of silicide formed over said layer of said second semiconductor.

5. (original) The integrated circuit of claim 1 wherein said first semiconductor consists essentially of a semiconductor selected from the group consisting of silicon, silicon germanium and silicon carbide and said second semiconductor consists essentially of another semiconductor different from said first semiconductor, said another semiconductor selected from the group consisting of silicon, silicon germanium and silicon carbide.

6. (original) The integrated circuit of claim 1 wherein said first semiconductor consists essentially of silicon and said second semiconductor consists essentially of silicon germanium.

7. (original) The integrated circuit of claim 1 wherein said first semiconductor consists essentially of silicon germanium according to a first formula $Si_{x1}Ge_{y1}$, where x1 and y1 are percentages, x1 + y1 = 100%, y1 being at least one percent and said second semiconductor consists essentially of silicon germanium according to a second formula

$Si_{x2}Ge_{y2}$, where x2 and y2 are percentages, x2 + y2 = 100%, y2 being at least one percent, wherein x1 is not equal to x2 and y1 is not equal to y2.

8. (original) The integrated circuit of claim 1 wherein said first stress is a compressive stress.

9. (original) The integrated circuit of claim 6 wherein said second semiconductor consists essentially of silicon germanium having a germanium content of at least one percent.

10. (currently amended) The integrated circuit of claim 4 wherein ~~each of said PFET and said NFET further comprise a~~ said layer of silicide ~~contacting~~ contacts said gate conductors, said source regions and said drain regions of said PFET and said NFET.

11. (original) An integrated circuit having complementary metal oxide semiconductor (CMOS) transistors including a p-type field effect transistor (PFET) and an n-type field effect transistor (NFET), each said NFET and said PFET having a channel region disposed in a single-crystal layer of a first semiconductor, wherein a first stress is applied to a channel region of said PFET but not to a channel region of said NFET by a layer of a second semiconductor lattice-mismatched to said first semiconductor being formed in raised source and drain regions of said PFET, said layer of said second semiconductor not being formed in raised source and drain regions of

said NFET.

12. (original) An integrated circuit having complementary metal oxide semiconductor (CMOS) transistors including a p-type field effect transistor (PFET) and an n-type field effect transistor (NFET) each having channel regions disposed in single-crystal silicon regions of a substrate wherein a first stress is applied to the channel region of the PFET but not to the channel region of the NFET via a raised lattice-mismatched semiconductor layer consisting essentially of silicon germanium disposed in source and drain regions of the PFET a first distance from said channel region of said PFET and disposed in source and drain regions of the NFET a second distance from said channel region of said NFET, said silicon germanium having a composition according to the formula Si_xGe_y where x and y are percentages each being at least one percent, x plus y equaling 100 percent.

13-28. (canceled)